HTS200N03 P-1

30V N-Ch Power MOSFET

V_{DS}		30	V
$R_{DS(on),typ}$	V_{GS}=10V	15.5	mΩ
$I_{D\ (Sillicon\ Limited)}$		9.5	A

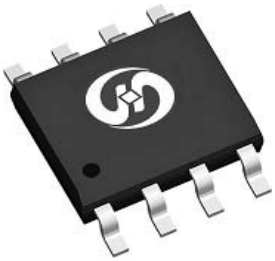
Feature

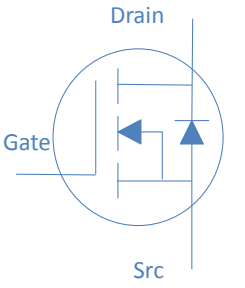
- ◇ High Speed Power Switching, Logic Level
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free

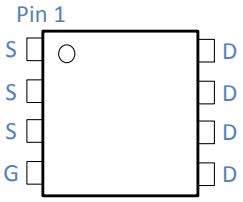
Application

- ◇ Hard Switching and High Speed Circuit
- ◇ DC/DC in Telecoms and Inductrial

SOIC-8







Part Number	Package	Marking
HTS200N03	SOIC-8	TS200N03

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_A=25℃	9.5	A
		T_A=70℃	7.5	
Drain to Source Voltage	V_{DS}	-	30	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	38	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	3.2	mJ
Power Dissipation	P_D	T_A=25℃	2.5	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	25	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	1.5	3	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=24V, T_j=25℃	-	-	1	μA
		V_{GS}=0V, V_{DS}=20V, T_j=125℃	-	-	25	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=8A	-	15.5	20	mΩ
		V_{GS}=4.5V, I_D=6A	-	25	30	
Transconductance	g_{fs}	V_{DS}=5V, I_D=8A	-	16	-	S
Gate Resistance	R_G	V_{GS}=15mV, V_{DS} =0V, f=1MHz	-	2.0	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	-	540	-	pF
Output Capacitance	C_{oss}		-	109	-	
Reverse Transfer Capacitance	C_{rss}		-	83	-	
Total Gate Charge	Q_g(10V)	V_{DD}=15V, I_D=8A, V_{GS}=10V	-	11.5	-	nC
	Q_g(4.5V)			6.1		
Gate to Source Charge	Q_{gs}		-	1.6	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.3	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=15V, I_D=1A, V_{GS}=10V, R_G=6Ω,	-	10	-	ns
Rise time	t_r		-	12	-	
Turn off Delay Time	$t_{d(off)}$		-	15	-	
Fall Time	t_f		-	10	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=2.3A	-		1.2	V
Reverse Recovery Time	t_{rr}	I_F=2.3A, dI_F/dt=100A/μs	-	20	-	ns
Reverse Recovery Charge	Q_{rr}		-	5	-	nC

Fig 1. Typical Output Characteristics

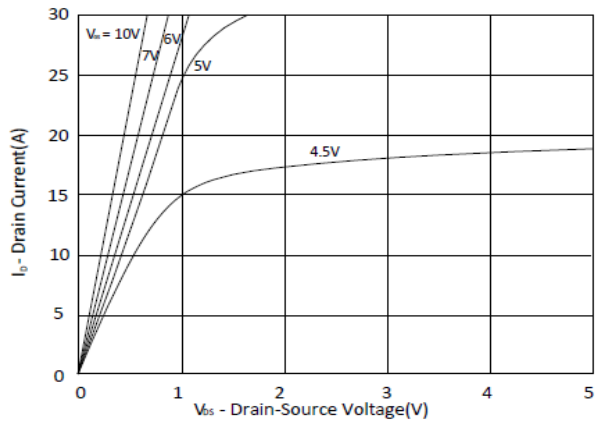


Figure 2. On-Resistance vs. Gate-Source Voltage

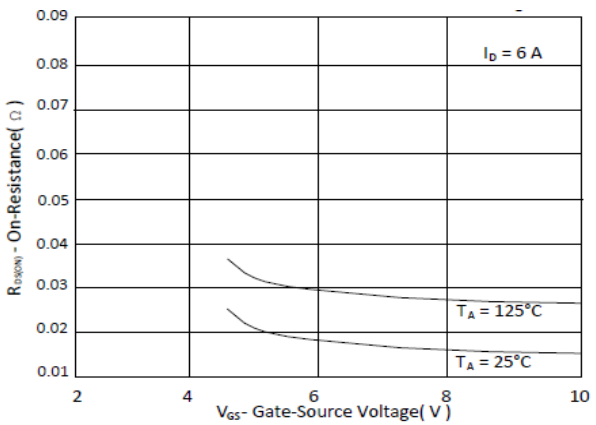


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

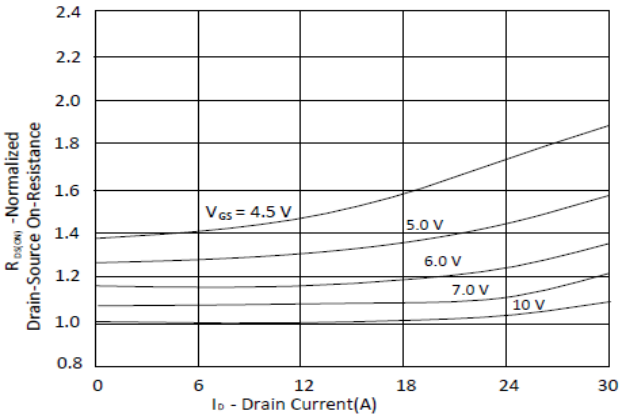


Figure 4. Normalized On-Resistance vs. Junction Temperature

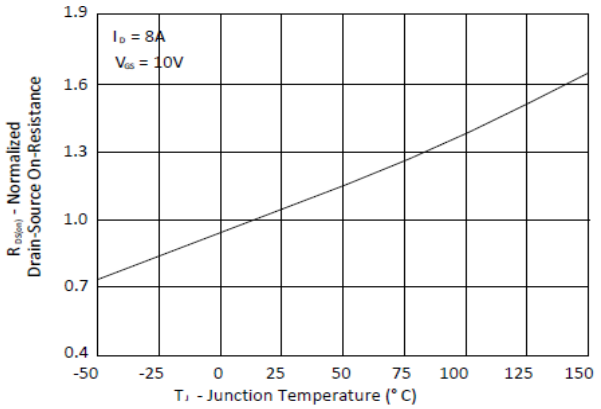


Figure 5. Typical Transfer Characteristics

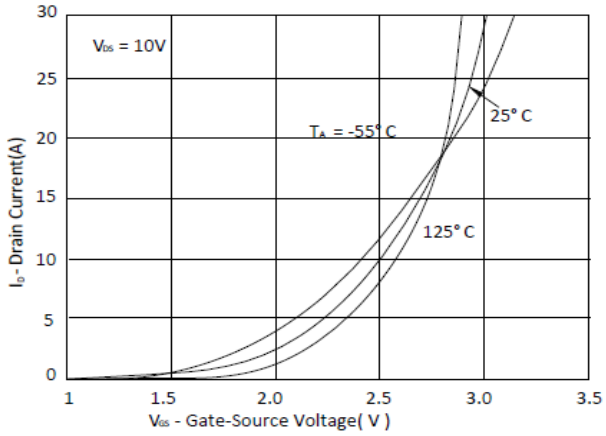


Figure 6. Typical Source-Drain Diode Forward Voltage

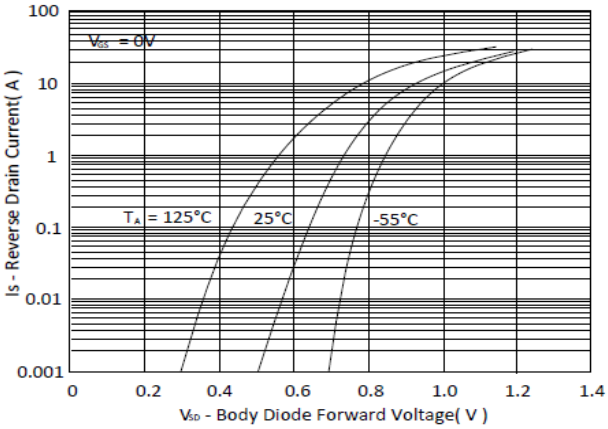


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

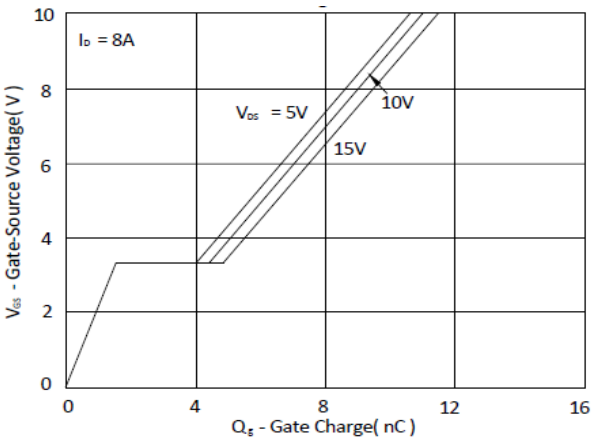


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

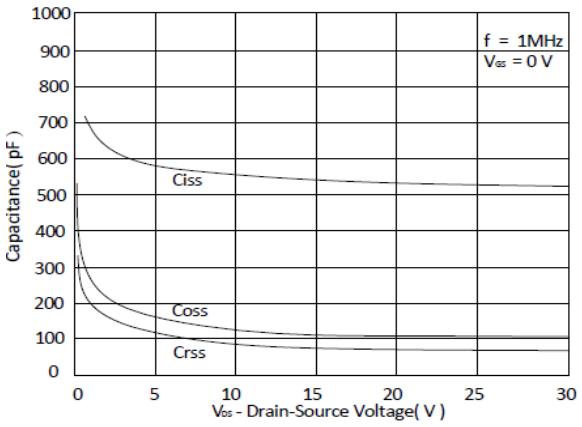


Figure 9. Maximum Safe Operating Area

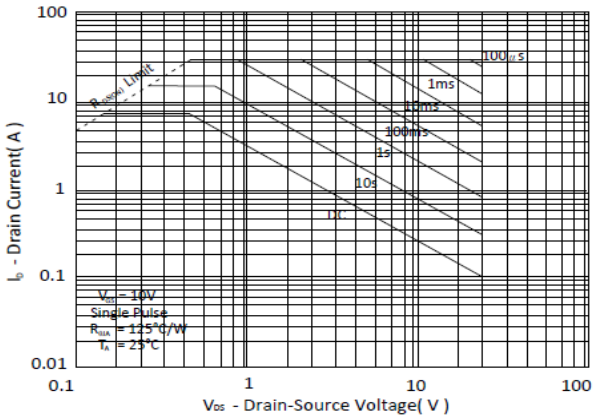


Figure 10. Single Pulse Maximum Power Dissipation

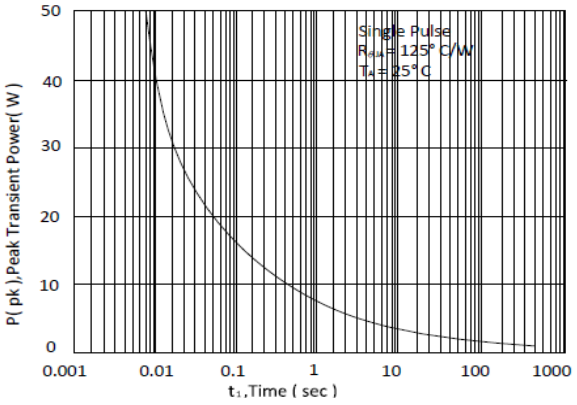
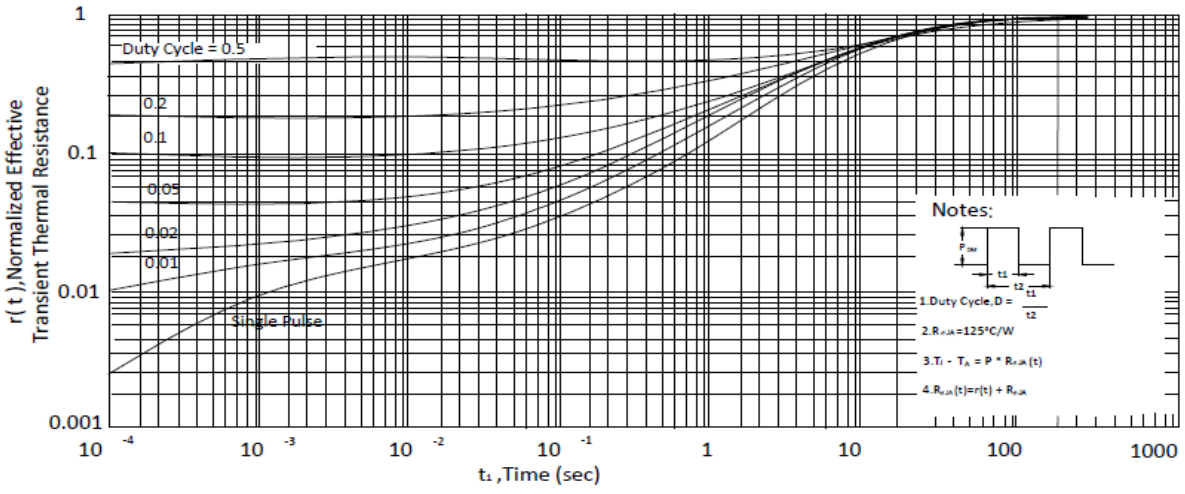
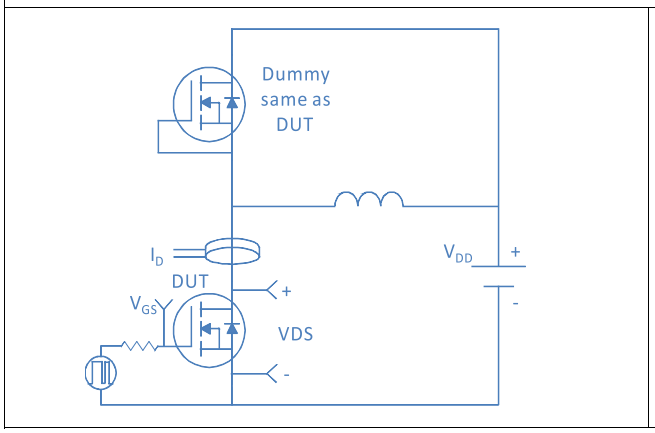
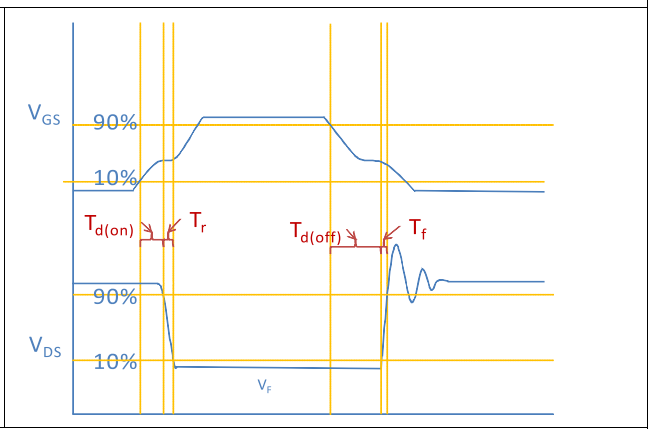


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

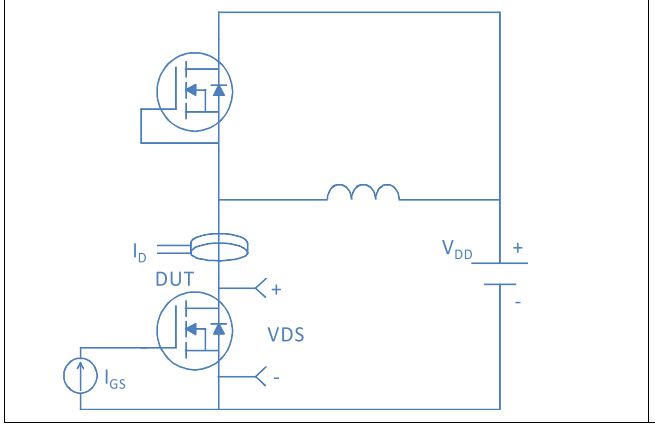


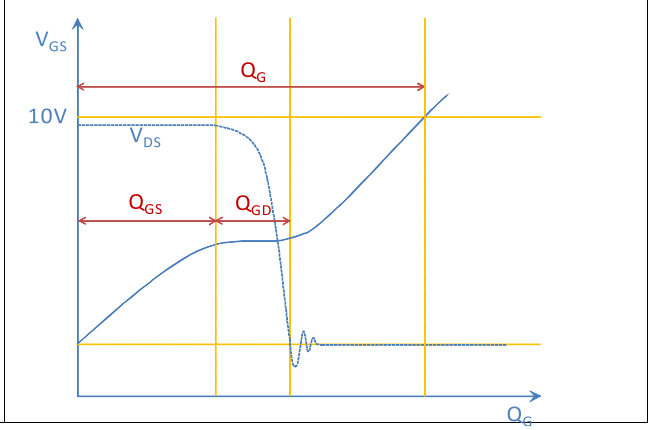
Inductive switching Test



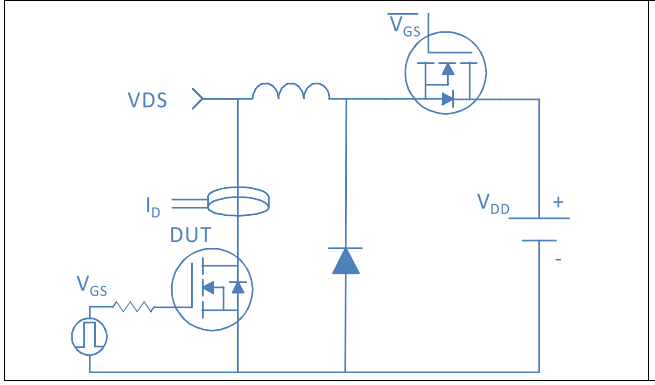


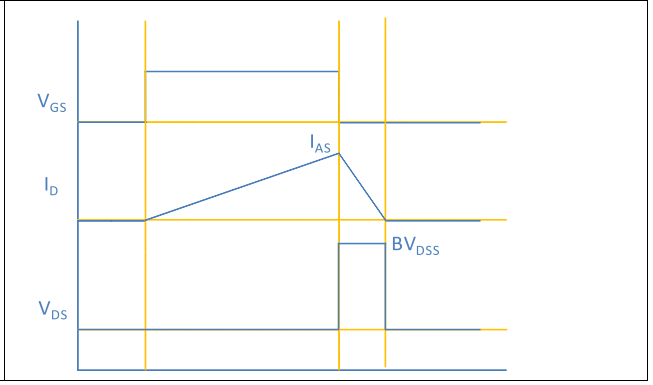
Gate Charge Test



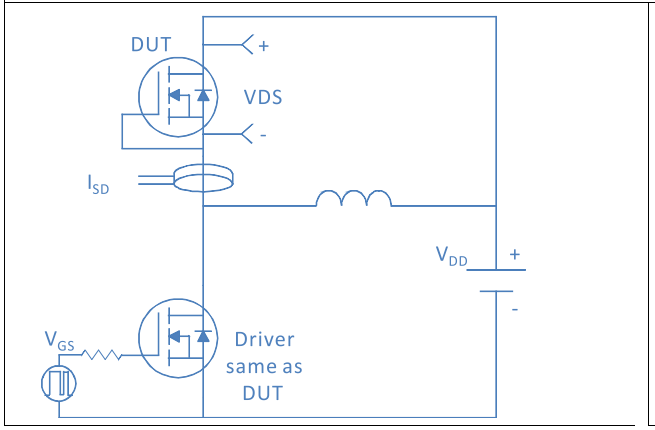


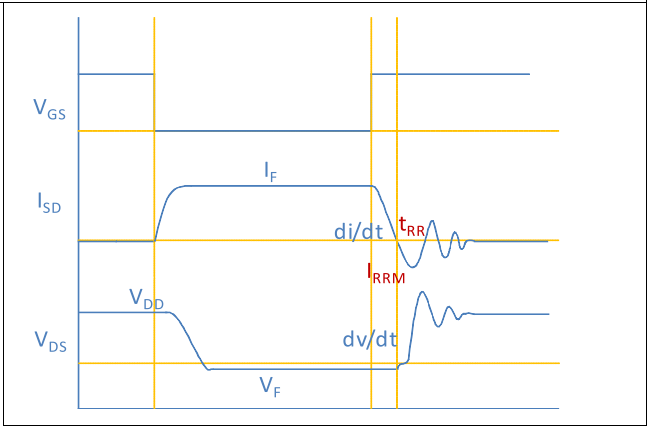
Uclamped Inductive Switching (UIS) Test





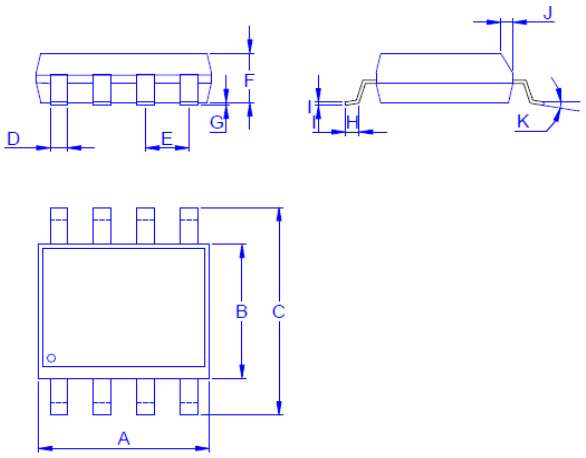
Diode Recovery Test





Package Outline

SOIC-8, 8 leads



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°